

FIG. 1A

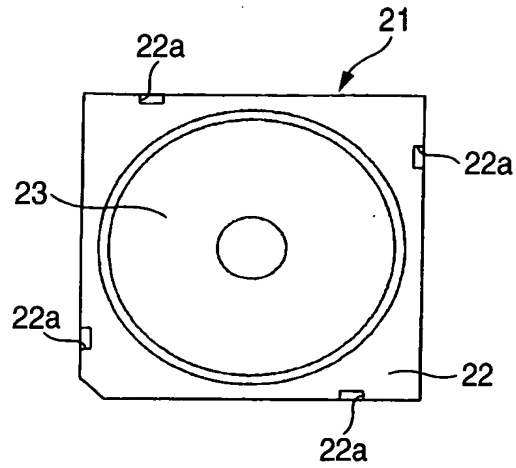


FIG. 1B

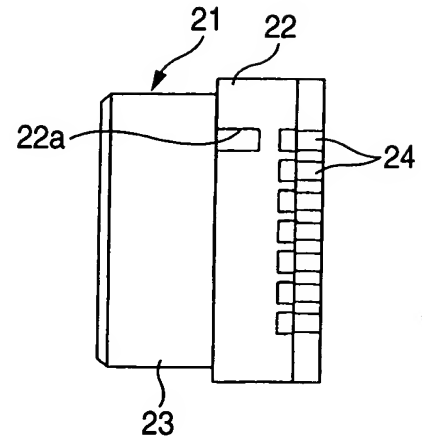


FIG. 1C

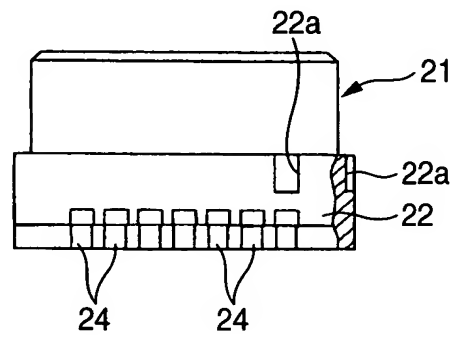


FIG. 1D

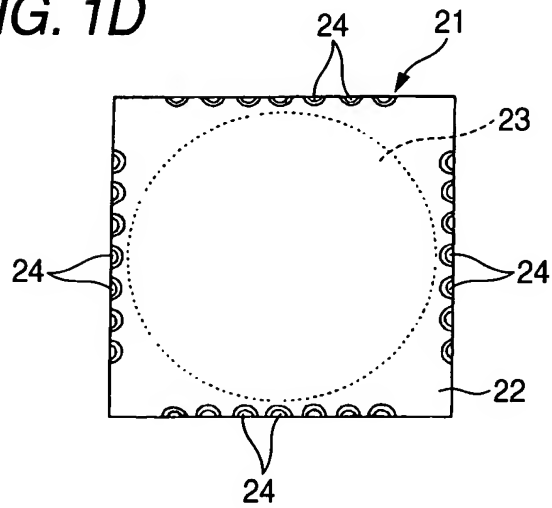


FIG. 2A

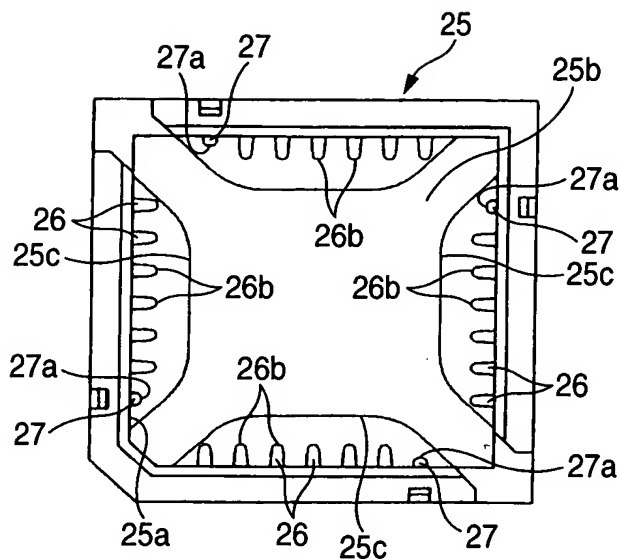


FIG. 2B

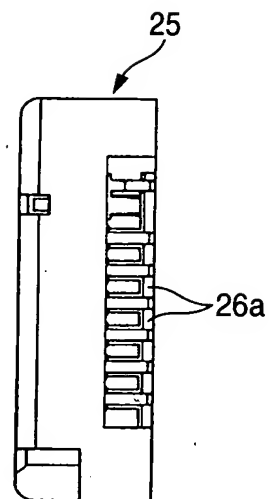


FIG. 2C

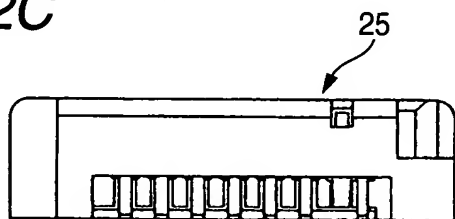


FIG. 2D

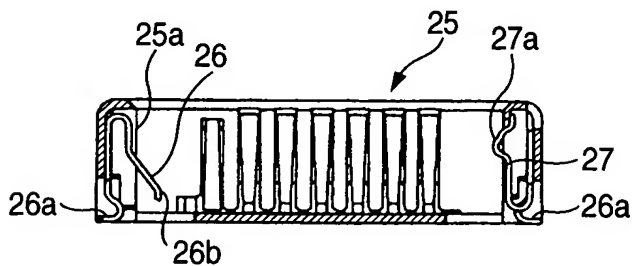


FIG. 3

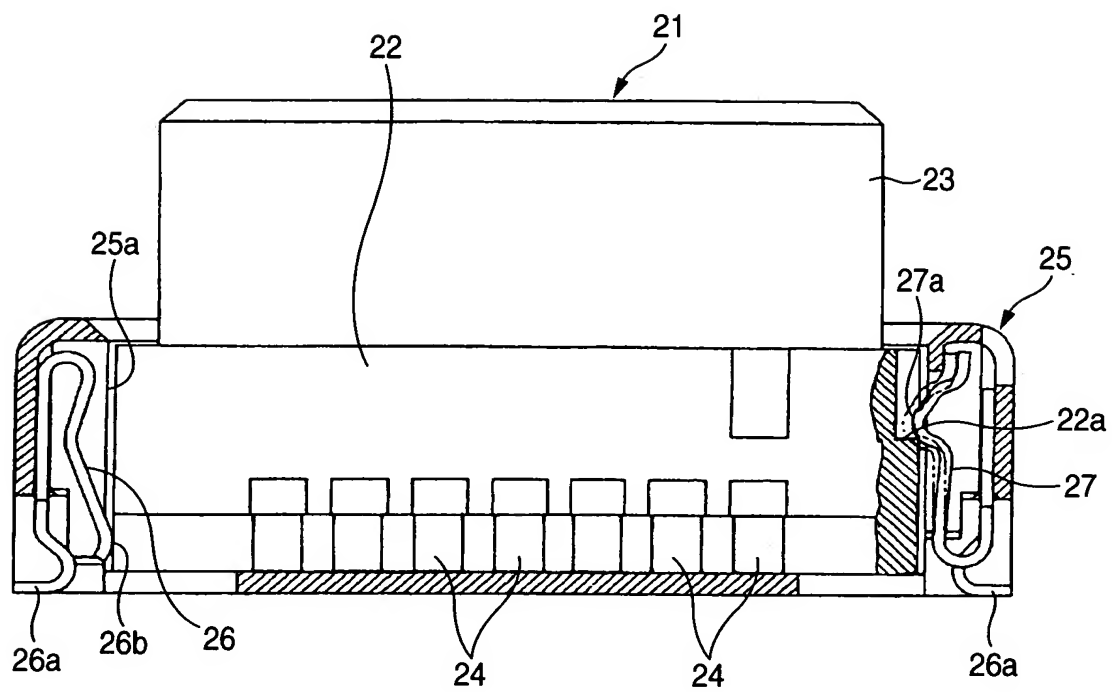


FIG. 4A

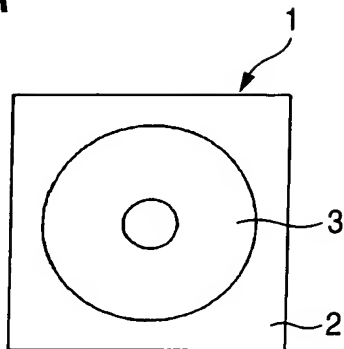


FIG. 4B

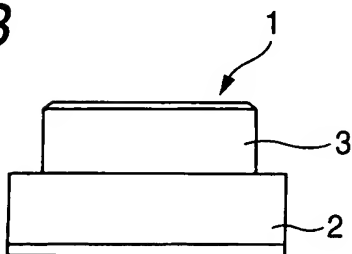


FIG. 4C

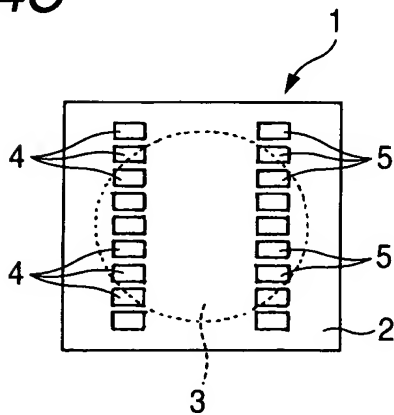


FIG. 1 is a perspective view of a rectangular substrate 6. The substrate 6 has a top surface 6b and a bottom surface 6c. A central rectangular opening 6a is formed in the substrate 6. The left and right side surfaces of the substrate 6 are labeled 9b and 10b, respectively.

This cross-sectional view shows a semiconductor device with a central channel region (9) and side regions (10). The channel region (9) is defined by a gate structure (9a) and is separated from the side regions (10) by a barrier layer (10a). The device is mounted on a substrate (6) with a base layer (6b). The channel region (9) is connected to a terminal (9b), and the side regions (10) are connected to a terminal (10b). The device is also connected to a terminal (7) and a terminal (8).

FIG. 7

